

1 CLAIMS
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3 1. A method including concurrently performing a plurality of memory
4 lookups in response to a sequence of inputs each having information;

5 each one of said memory lookups being performed in response to a corre-
6 sponding distinct one of said inputs;

7 each one of said memory lookups being performed at a corresponding
8 memory;

9 whereby each one of said sequence of inputs has a memory lookup per-
10 formed by an associated said memory for at least some of said information.

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12 2. A method as in claim 1, including substantially concurrently pro-
13 viding results responsive to a plurality of said inputs accessing different subsequences of
14 said memories.

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16 3. A method as in claim 1, wherein at least some inputs have their in-
17 formation applied to all said memories at least once, and to at least some of said memo-
18 ries at least twice.

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20 4. A method as in claim 1, wherein each one of said memory lookups is
21 performed in response to a portion of said information.

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1 5. A method as in claim 1, wherein each said input has substantially
2 equal amounts of said information.

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4 6. A method as in claim 1, wherein said memory lookups are each sub-
5 stantially performed on a single monolithic integrated circuit.

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7 7. A method as in claim 1, wherein said sequence of inputs includes at
8 least one of: a destination IP address, an IP address, packet header information.

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10 8. A method as in claim 1, wherein said corresponding memories col-
11 lectively include lookup results including at least one datum responsive to each one of
12 said inputs.

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14 9. A method as in claim 8, wherein said lookup results collectively in-
15 clude packet forwarding information.

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17 10. A method as in claim 1, wherein said memory lookup includes a se-
18 quence of individual memory accesses, each said individual memory access being per-
19 formed at one of said memories.

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1 11. A method as in claim 10, including substantially concurrently pro-
2 viding results responsive to a plurality of said inputs accessing different subsequences of
3 said memories.

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5 12. A method as in claim 10, wherein at least some inputs have their in-
6 formation applied to all said memories at least once, and to at least some of said memo-
7 ries at least twice.

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9 13. A method as in claim 10, wherein each said input has substantially
10 equal amounts of said information.

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12 14. A method as in claim 10, wherein said sequence of individual mem-
13 ory accesses includes one said individual memory access at each said memory.

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15 15. A method as in claim 10, wherein said sequence of individual mem-
16 ory accesses includes one said individual memory access at each said memory, followed
17 by a second individual memory access at each said memory for at least a subsequence of
18 said memories.

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20 16. A method as in claim 10, wherein said sequence of individual mem-
21 ory accesses includes one said individual memory access at each said memory for only a
22 subsequence of said memories.

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2 17. A method including
3 coupling each one of a sequence of inputs to a sequence of memories, said
4 sequence having a last memory and a next memory corresponding to each said memory
5 other than said last memory, wherein each said memory is responsive to a distinct portion
6 of said information;

7 coupling a result from each said memory other than said last memory to its
8 corresponding said next memory in said sequence; and

9 providing an output of at least one of said memories;
10 whereby said sequence of inputs is each coupled to said sequence of memo-
11 ries in a pipelined manner to provide said output at a rate substantially equaling one out-
12 put as each input is received.

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14 18. A method as in claim 17, including substantially concurrently pro-
15 viding results responsive to a plurality of said inputs accessing different subsequences of
16 said memories.

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18 19. A method as in claim 17, wherein at least some inputs have their in-
19 formation applied to all said memories at least once, and to at least some of said memo-
20 ries at least twice.

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1 20. A method as in claim 17, wherein each said input has substantially
2 equal amounts of said information.

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4 21. A method as in claim 17, wherein said sequence of inputs includes at
5 least one of: a destination IP address, an IP address, packet header information.

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7 22. A method as in claim 17, wherein said sequence of memories are
8 substantially included in a single monolithic integrated circuit.

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10 23. A method as in claim 17, wherein said output is responsive to a se-
11 quence of individual memory accesses, each said individual memory access being per-
12 formed at one of said memories.

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14 24. A method as in claim 23, wherein at least some inputs have their in-
15 formation applied to all said memories at least once, and to at least some of said memo-
16 ries at least twice.

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18 25. A method as in claim 23, wherein said sequence of individual mem-
19 ory accesses includes one said individual memory access at each said memory.

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21 26. A method as in claim 23, wherein said sequence of individual mem-
22 ory accesses includes one said individual memory access at each said memory, followed

1 by a second individual memory access at each said memory for at least a subsequence of
2 said memories.

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4 27. A method as in claim 23, wherein said sequence of individual mem-
5 ory accesses includes one said individual memory access at each said memory for only a
6 subsequence of said memories.

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8 28. A method as in claim 17, wherein said sequence of memories col-
9 lectively include lookup results including at least one datum responsive to each one of
10 said inputs.

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12 29. A method as in claim 28, wherein said lookup results collectively in-
13 clude a set of packet forwarding information.

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15 30. Apparatus including a circuit integrated onto a monolithic semicon-
16 ductor chip, said circuit including

17 a sequence of registers each having a portion of a corresponding lookup
18 search key in a sequence of said lookup search keys, each said register coupled to a cor-
19 responding one of a sequence of on-chip memories;

20 a subsequence of said memories not including a last said memory each
21 having an output register associated therewith, said output register being coupled to an
22 associated next said memory for each said memory in said subsequence;

1 a plurality of said memories capable of operating substantially concurrently
2 each on a portion of a corresponding plurality of said lookup search keys;
3 whereby said sequence of registers is capable of coupling each lookup
4 search key in portions to said sequence of memories, each said memory being responsive
5 to each said lookup search key in sequence, each said lookup search key being coupled to
6 each said memory in sequence.

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8 31. Apparatus as in claim 30, including an output register associated
9 with said last memory and coupled to an output of said apparatus.

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11 32. Apparatus as in claim 30, including an output register associated
12 with said last memory, said output register being coupled to an associated earlier memory
13 in said sequence.

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15 33. Apparatus as in claim 30, wherein a plurality of output registers as-
16 sociated with different memories are each coupled to an output for said circuit.

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18 34. Apparatus as in claim 30, wherein an output register associated with
19 a memory other than said last memory is coupled to an output for said circuit.

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21 35. Apparatus as in claim 30, wherein said lookup search key includes at
22 least one of: a destination IP address, an IP address, packet header information.

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2 36. Apparatus as in claim 30, wherein said memories collectively in-
3 clude lookup results including at least one datum responsive to each one of said inputs.

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5 37. Apparatus as in claim 36, wherein said lookup results collectively
6 include packet forwarding information.

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8 38. Apparatus including
9 a sequence of memories, said sequence having a last memory and a next
10 memory corresponding to each said memory other than said last memory, each said
11 memory being coupled to a distinct portion of one of a sequence of lookup search keys;
12 each said memory other than said last memory being coupled to its corre-
13 sponding said next memory in said sequence; and
14 whereby said sequence of inputs is each coupled to said sequence of memo-
15 ries in a pipelined manner to provide said output at a rate substantially equaling one out-
16 put as each input is received.

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18 39. Apparatus as in claim 38, wherein a plurality of output registers as-
19 sociated with different memories are each coupled to an output for said circuit.

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21 40. Apparatus as in claim 38, wherein an output register associated with
22 a memory other than said last memory is coupled to an output for said circuit.

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2 41. Apparatus as in claim 38, wherein said last memory is coupled to an
3 associated earlier memory in said sequence.

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5 42. Apparatus as in claim 38, wherein said sequence of lookup search
6 keys includes at least one of: a destination IP address, an IP address, packet header in-
7 formation.

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9 43. Apparatus as in claim 38, wherein said sequence of memories col-
10 lectively include lookup results including at least one datum responsive to each one of
11 said lookup search keys.

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13 44. Apparatus as in claim 43, wherein said lookup results collectively
14 include a set of packet forwarding information.